REMARKS

Prior to the present response, claims 1-3, 6-8, 11-15 and 18-20 were pending in the present application, and remain pending after the present response. Reconsideration and allowance of outstanding claims 1-3, 6-8, 11-15 and 18-20 in view of the following remarks are respectfully requested.

A. Rejections of Claims 1-3, 6-8, 11-15 and 18-20 under 35 USC §102(e)

The Examiner has rejected claims 1-3, 6-8, 11-15 and 18-20 under 35 USC §102(e) as being anticipated by U.S. Patent Application Publication Number US 2001/0042190 to Tremblay, et al. ("Tremblay"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 1, 7, 11, and 19, is patentably distinguishable over Tremblay.

As disclosed in the present application, conventional approaches in the processor architecture field do not adequately address the problem of consumption of chip area for wide buses, such as wide "move" buses linking various register file banks. Various embodiments according to the present invention address and overcome the need in the art for speeding up the very long instruction word ("VLIW") processor architecture and reducing power consumption and reducing chip area while accommodating multiple register file banks and multiple execution units.

Embodiments according to the present invention, as shown in Figure 2 of the present application, include first and second register file banks. The first register file

bank comprises a first plurality of read ports and write ports, and the second register file bank comprises a second plurality of read ports and write ports. A first data path block comprises a first plurality of execution units, and a second data path block comprises a second plurality of execution units. A first plurality of buses couple the first plurality of read ports to each of the first and second data path blocks. A second plurality of buses couple the second plurality of read ports to each of the first and second data path blocks. An operand residing in the first plurality of read ports is concurrently accessed by the first plurality of execution units in the first data path block and by the second plurality of execution units in the second data path block. In addition, a result of an operation performed in the first data path block is written to only the first plurality of write ports of the first register file bank without being written to the second plurality of write ports of the second register file bank.

In contrast, the VLIW processor in Tremblay includes a plurality of functional units and a multi-ported register file that is divided into a plurality of separate register file segments. See, for example, Tremblay, paragraph 0011, lines 1-4. Furthermore, as seen in Figure 2, a separate register file segment 224 is allocated to each of the media functional units 220 and general functional unit 222. See, for example, Tremblay, paragraph 0039, lines 6-8. The VLIW processor in Tremblay, however, "partitions the register file into local and global registers." See Tremblay, paragraph 63, lines 1-2. In addition, the "global registers are read and written by all functional units 620, 622, 624, and 626" while the "local registers are read and written only by a functional unit

associated with a particular register file segment." See Tremblay, paragraph 64, lines 13-16.

The Examiner, in the present final office action, refers to the local and global registers in Tremblay as being one and the same to reject claims 1-3, 6-8, 11-15 and 18-20 of the present invention. See for example, the present final office action, page 11, lines 8-12 and page 12, lines 9-11. Applicants respectfully submit that the local and global registers cannot be treated as such because Tremblay explains that the global and local registers are "distinct and independent." See Tremblay, paragraph 14, lines 2-6. According to Tremblay, the "[l]ocal registers allocated to a functional unit are not accessible or 'visible' to other functional units." See Tremblay, paragraph 39, lines 17-18. Thus, as further seen in Figure 6 of Tremblay, each local register is readable only by its associated functional unit. In the present invention, however, as seen in Figure 2 for example, register file bank 252 can be read (is accessible) by either data path block 212 or 214. See, for example, the present application, page 15, line 22 through page 16, line 5:

> "[A]ccording to the present invention, the operands residing in each register file bank 252 and 254 are readily available to either data path block 212 or 214 without the requirement of a time consuming move operation. In other words, according to the present invention, operands residing in register file banks 252 and 254 are equally accessible to either data path block 212 or data path block 214."

Tremblay, therefore, does not teach, disclose, or suggest the configuration in the present invention especially since, for example, according to the VLIW processor of Tremblay, the register file is partitioned into distinct and independent registers.

Therefore, Applicants respectfully submit that the VLIW processor in Tremblay, with its partitioned register file configuration, does not teach, disclose, or suggest a VLIW processor wherein an operand residing in a first plurality of read ports is *concurrently* accessed by a first plurality of execution units in a first data path block and by a second plurality of execution units in a second data path block.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by independent claims 1, 7, 11, and 19 is not taught, disclosed, or suggested by the art of record. As such, the claims depending from independent claims 1, 7, 11, and 19 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 7, 11, and 19, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-3, 6-8, 11-15 and 18-20 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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